WHAT IS CLAIMED IS:

1. A ferroelectric capacitor, comprising:

a first electrode layer located over a substrate, wherein the first electrode layer includes iridium;

an oxide electrode template located over the first electrode layer;

a ferroelectric dielectric layer located over the oxide electrode template; and

a second electrode layer located over the ferroelectric dielectric layer.

2. The ferroelectric capacitor as recited in Claim 1 wherein the oxide electrode template forms a portion of a first electrode.

3. The ferroelectric capacitor as recited in Claim 1 wherein the oxide electrode template comprises a perovskite material.

4. The ferroelectric capacitor as recited in Claim 1 wherein the oxide electrode template comprises a distorted perovskite material.

5. The ferroelectric capacitor as recited in Claim 1 wherein the oxide electrode template is selected from the group consisting

of $SrIrO_3$ and SrRuO3.

6. The ferroelectric capacitor as recited in Claim 1 wherein the oxide electrode template is selected from the group consisting of $BaPbO_3$, $PbIrO_3$, $PbRuO_3$, $BiRuO_3$, $BiIrO_3$, $(La,Sr)CoO_3$, $CaRuO_3$, and $BaPbO_3$.

7. The ferroelectric capacitor as recited in Claim 1 wherein the oxide electrode template has a thickness ranging from about 20 nm to about 100 nm.

8. The ferroelectric capacitor as recited in Claim 1 wherein the oxide electrode template has a resistivity less than about 400 micro-ohms/cm.

9. The ferroelectric capacitor as recited in Claim 1 wherein the oxide electrode template and the ferroelectric dielectric layer have substantially similar crystal structures.

10. The ferroelectric capacitor as recited in Claim 1 wherein the oxide electrode template is a first oxide electrode template and further including a second oxide electrode template located between the ferroelectric dielectric layer and the second electrode layer.

11. A method for manufacturing a ferroelectric capacitor, comprising:

forming a first electrode layer over a substrate;

forming an oxide electrode template over the first electrode layer;

forming a ferroelectric dielectric layer over the oxide electrode template; and

forming a second electrode layer over the ferroelectric dielectric layer, wherein the ferroelectric capacitor is formed only using temperatures of about 500°C or less.

12. The method as recited in Claim 11 wherein forming an oxide electrode template includes forming an oxide electrode template comprising a perovskite material.

13. The method as recited in Claim 11 wherein forming an oxide electrode template includes forming an oxide electrode template comprising a distorted perovskite material.

14. The method as recited in Claim 11 wherein forming an oxide electrode template includes forming an oxide electrode template comprising a material selected from the group consisting of $SrIrO_3$ and $SrRuO_3$.

15. The method as recited in Claim 11 wherein forming an oxide electrode template includes forming an oxide electrode template comprising a material selected from the group consisting of $BaPbO_3$, $PbIrO_3$, $PbRuO_3$, $BiRuO_3$, $BiIrO_3$, $(La,Sr)CoO_3$, $CaRuO_3$, and $BaPbO_3$.

16. The method as recited in Claim 11 wherein forming an oxide electrode template includes forming an oxide electrode template having a thickness ranging from about 20 nm to about 100 nm.

17. The method as recited in Claim 11 wherein forming an oxide electrode template includes forming an oxide electrode template having a resistivity less than about 400 micro-ohms/cm.

18. The method as recited in Claim 11 wherein forming an oxide electrode template and forming a ferroelectric dielectric layer includes forming an oxide electrode template and forming a ferroelectric dielectric layer having substantially similar crystal structures.

19. The method as recited in Claim 11 wherein forming an oxide electrode template includes forming a first oxide electrode template and further including forming a second oxide electrode

template between the ferroelectric dielectric layer and the second electrode layer.

20. The method as recited in Claim 11 wherein the first electrode layer is an iridium electrode layer.

21. A ferroelectric random access memory (FeRAM) device, comprising:

a transistor having source/drain regions located over a semiconductor substrate;

an interlevel dielectric layer located over the transistor, the interlevel dielectric layer having a conductive plug therein contacting at least one of the source/drain regions; and

a ferroelectric capacitor located over the interlevel dielectric layer and contacting the conductive plug, including;

a first electrode layer located over the interlevel dielectric layer, wherein the first electrode layer includes iridium;

an oxide electrode template located over the first electrode layer;

a ferroelectric dielectric layer located over the oxide electrode template; and

a second electrode layer located over the ferroelectric dielectric layer.

22. The ferroelectric random access memory (FeRAM) device as recited in Claim 21 wherein at least a portion of the transistor includes a nickel silicide.